JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for MTECH II Semester (R16 / R13) Regular / Supplementary Examinations, JULY - 2019.

College: VASIREDDY VENKATADRI INST. OF TECHNOLOGY, NUMBURU, GUNTUR:BQ

Discrepancy pertaining to these results are to be submitted on or before 09-11-2019 with following documents at CE Office,JNTUK,Kakinada

Htno	Subcode	Subname	Internal	External	credits
15BQ1D5408	H4308	SPECIAL MACHINES ELECTIVE-IV	35	30	1
15BQ1D5806	H0501	DATA WAREHOUSING AND DATA MINING	30	-1	0
16BQ1D5805	J4001	ADVANCED UNIX PROGRAMMING	32	24	1
16BQ1D5805	J5801	COMPUTER NETWORKS	29	28	1
17BQ1D1501	J1501	OPTIMIZATION AND RELIABILITY	32	7	0
17BQ1D1501	J1503	DESIGN WITH ADVANCED MATERIALS	30	28	1
17BQ1D1501	J1509	MECHATRONICS ELECTIVE-IV	28	7	0
17BQ1D5802	J0502	SOFTWARE ENGINEERING ELECTIVE I	24	9	0
17BQ1D5802	J2503	CYBER SECURITY	30	24	1
17BQ1D5802	J4001	ADVANCED UNIX PROGRAMMING	34	25	1
17BQ1D5802	J4002	BIG DATA ANALYTICS	26	31	1
17BQ1D8704	J8703	STABILITY OF STRUCTURES	31	28	1
17BQ1D8705	J8703	STABILITY OF STRUCTURES	31	20	0
18BQ1D1501	J1501	OPTIMIZATION AND RELIABILITY	40	26	1
18BQ1D1501	J1502	EXPERIMENTAL STRESS ANALYSIS	33	32	1
18BQ1D1501	J1503	DESIGN WITH ADVANCED MATERIALS	40	36	1
18BQ1D1501	J1504	TRIBOLOGY ELECTIVE-III	34	35	1
18BQ1D1501	J1509	MECHATRONICS ELECTIVE-IV	33	24	1
18BQ1D1501	J1511	DESIGN PRACTICE LAB	38	54	1
18BQ1D1501	J2103	FINITE ELEMENT METHODS	37	0	0
18BQ1D1502	J1501	OPTIMIZATION AND RELIABILITY	37	29	1
18BQ1D1502	J1502	EXPERIMENTAL STRESS ANALYSIS	29	-1	0
18BQ1D1502	J1503	DESIGN WITH ADVANCED MATERIALS	39	39	1
18BQ1D1502	J1504	TRIBOLOGY ELECTIVE-III	37	-1	0
18BQ1D1502	J1509	MECHATRONICS ELECTIVE-IV	31	-1	0
18BQ1D1502	J1511	DESIGN PRACTICE LAB	35	55	1
18BQ1D1502	J2103	FINITE ELEMENT METHODS	37	0	0
18BQ1D5801	J0502	SOFTWARE ENGINEERING ELECTIVE I	36	24	1
18BQ1D5801	J2503	CYBER SECURITY	36	30	1
18BQ1D5801	J2510	CLOUD COMPUTING ELECTIVE II	34	35	1
18BQ1D5801	J4001	ADVANCED UNIX PROGRAMMING	36	24	1
18BQ1D5801	J4002	BIG DATA ANALYTICS	35	27	1
18BQ1D5801	J5801	COMPUTER NETWORKS	37	28	1
18BQ1D5801	J5803	CSE LAB 2	38	56	1
18BQ1D5802	J0502	SOFTWARE ENGINEERING ELECTIVE I	30	24	1
18BQ1D5802	J2503	CYBER SECURITY	34	33	1
18BQ1D5802	J2510	CLOUD COMPUTING ELECTIVE II	36	30	1
18BQ1D5802	J4001	ADVANCED UNIX PROGRAMMING	38	24	1
18BQ1D5802	J4002	BIG DATA ANALYTICS	37	35	1
18BQ1D5802	J5801	COMPUTER NETWORKS	38	30	1
18BQ1D5802	J5803	CSE LAB 2	37	56	1

Htno	Subcode	Subname	Internal	External	credits
18BQ1D5803	J0502	SOFTWARE ENGINEERING ELECTIVE I	40	32	1
18BQ1D5803	J2503	CYBER SECURITY	40	31	1
18BQ1D5803	J2510	CLOUD COMPUTING ELECTIVE II	40	31	1
18BQ1D5803	J4001	ADVANCED UNIX PROGRAMMING	39	28	1
18BQ1D5803	J4002	BIG DATA ANALYTICS	40	41	1
18BQ1D5803	J5801	COMPUTER NETWORKS	40	31	1
18BQ1D5803	J5803	CSE LAB 2	40	58	1
18BQ1D5804	J0502	SOFTWARE ENGINEERING ELECTIVE I	34	10	0
18BQ1D5804	J2503	CYBER SECURITY	35	24	1
18BQ1D5804	J2510	CLOUD COMPUTING ELECTIVE II	34	26	1
18BQ1D5804	J4001	ADVANCED UNIX PROGRAMMING	39	24	1
18BQ1D5804	J4002	BIG DATA ANALYTICS	39	24	1
18BQ1D5804	J5801	COMPUTER NETWORKS	29	27	1
18BQ1D5804	J5803	CSE LAB 2	36	57	1
18BQ1D5805	J0502	SOFTWARE ENGINEERING ELECTIVE I	38	24	1
18BQ1D5805	J2503	CYBER SECURITY	33	28	1
18BQ1D5805	J2510	CLOUD COMPUTING ELECTIVE II	37	27	1
18BQ1D5805	J4001	ADVANCED UNIX PROGRAMMING	38	25	1
18BQ1D5805	J4002	BIG DATA ANALYTICS	39	34	1
18BQ1D5805	J5801	COMPUTER NETWORKS	35	25	1
18BQ1D5805	J5803	CSE LAB 2	38	56	1
18BQ1D5806	J0502	SOFTWARE ENGINEERING ELECTIVE I	39	27	1
18BQ1D5806	J2503	CYBER SECURITY	35	24	1
18BQ1D5806	J2510	CLOUD COMPUTING ELECTIVE II	38	28	1
18BQ1D5806	J4001	ADVANCED UNIX PROGRAMMING	36	28	1
18BQ1D5806	J4002	BIG DATA ANALYTICS	38	38	1
18BQ1D5806	J5801	COMPUTER NETWORKS	39	30	1
18BQ1D5806	J5803	CSE LAB 2	38	58	1
18BQ1D5807	J0502	SOFTWARE ENGINEERING ELECTIVE I	40	27	1
18BQ1D5807	J2503	CYBER SECURITY	33	34	1
18BQ1D5807	J2510	CLOUD COMPUTING ELECTIVE II	37	32	1
18BQ1D5807	J4001	ADVANCED UNIX PROGRAMMING	35	24	1
18BQ1D5807	J4002	BIG DATA ANALYTICS	39	40	1
18BQ1D5807	J5801	COMPUTER NETWORKS	38	30	1
18BQ1D5807	J5803	CSE LAB 2	40	57	1
18BQ1D8701	J8701	FINITE ELEMENT METHODS	27	33	1
18BQ1D8701	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	28	26	1
18BQ1D8701	J8703	STABILITY OF STRUCTURES	31	27	1
18BQ1D8701	J8704	THEORY OF PLATES & SHELLS	29	35	1
18BQ1D8701	J8705	PRESTRESSED CONCRETE ELECTIVEI	27	24	1
18BQ1D8701	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	28	32	1
18BQ1D8701	J8711	CAD LABORATORY	30	43	1
18BQ1D8702	J8701	FINITE ELEMENT METHODS	33	28	1
18BQ1D8702	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	27	32	1
18BQ1D8702	J8703	STABILITY OF STRUCTURES	31	24	1
18BQ1D8702	J8704	THEORY OF PLATES & SHELLS	31	15	0
18BQ1D8702	J8705	PRESTRESSED CONCRETE ELECTIVEI	30	11	0
18BQ1D8702	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	29	25	1
18BQ1D8702	J8711	CAD LABORATORY	32	53	1
18BQ1D8703	J8701	FINITE ELEMENT METHODS	36	39	1
18BQ1D8703	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	32	24	1

Htno	Subcode	Subname	Internal	External	credits
18BQ1D8703	J8703	STABILITY OF STRUCTURES	38	28	1
18BQ1D8703	J8704	THEORY OF PLATES & SHELLS	34	35	1
18BQ1D8703	J8705	PRESTRESSED CONCRETE ELECTIVEI	28	8	0
18BQ1D8703	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	27	28	1
18BQ1D8703	J8711	CAD LABORATORY	32	44	1
18BQ1D8704	J8701	FINITE ELEMENT METHODS	30	39	1
18BQ1D8704	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	30	38	1
18BQ1D8704	J8703	STABILITY OF STRUCTURES	36	26	1
18BQ1D8704	J8704	THEORY OF PLATES & SHELLS	31	26	1
18BQ1D8704	J8705	PRESTRESSED CONCRETE ELECTIVEI	30	14	0
18BQ1D8704	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	30	24	1
18BQ1D8704	J8711	CAD LABORATORY	28	48	1
18BQ1D8705	J8701	FINITE ELEMENT METHODS	38	45	1
18BQ1D8705	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	33	28	1
18BQ1D8705	J8703	STABILITY OF STRUCTURES	39	28	1
18BQ1D8705	J8704	THEORY OF PLATES & SHELLS	32	41	1
18BQ1D8705	J8705	PRESTRESSED CONCRETE ELECTIVEI	30	24	1
18BQ1D8705	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	35	38	1
18BQ1D8705	J8711	CAD LABORATORY	33	60	1
18BQ1D8706	J8701	FINITE ELEMENT METHODS	32	40	1
18BQ1D8706	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	34	24	1
18BQ1D8706	J8703	STABILITY OF STRUCTURES	34	24	1
18BQ1D8706	J8704	THEORY OF PLATES & SHELLS	28	36	1
18BQ1D8706	J8705	PRESTRESSED CONCRETE ELECTIVEI	30	12	0
18BQ1D8706	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	30	24	1
18BQ1D8706	J8711	CAD LABORATORY	30	50	1
18BQ1D8707	J8701	FINITE ELEMENT METHODS	35	41	1
18BQ1D8707	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	35	40	1
18BQ1D8707	J8703	STABILITY OF STRUCTURES	40	31	1
18BQ1D8707	J8704	THEORY OF PLATES & SHELLS	37	37	1
18BQ1D8707	J8705	PRESTRESSED CONCRETE ELECTIVEI	36	26	1
18BQ1D8707	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	34	42	1
18BQ1D8707	J8711	CAD LABORATORY	38	59	1
18BQ1D8708	J8701	FINITE ELEMENT METHODS	29	26	1
18BQ1D8708	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	30	24	1
18BQ1D8708	J8703	STABILITY OF STRUCTURES	28	24	1
18BQ1D8708	J8704	THEORY OF PLATES & SHELLS	30	25	1
18BQ1D8708	J8705	PRESTRESSED CONCRETE ELECTIVEI	28	20	0
18BQ1D8708	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	31	16	0
18BQ1D8708	J8711	CAD LABORATORY	38	59	1
18BQ1D8709	J8701	FINITE ELEMENT METHODS	27	37	1
18BQ1D8709	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	33	24	1
18BQ1D8709	J8703	STABILITY OF STRUCTURES	33	24	1
18BQ1D8709	J8704	THEORY OF PLATES & SHELLS	29	35	1
18BQ1D8709	J8705	PRESTRESSED CONCRETE ELECTIVEI	27	15	0
18BQ1D8709	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	30	24	1
18BQ1D8709	J8711	CAD LABORATORY	32	40	1
18BQ1D8710	J8701	FINITE ELEMENT METHODS	31	42	1
18BQ1D8710	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	29	24	1
18BQ1D8710	J8703	STABILITY OF STRUCTURES	32	27	1
18BQ1D8710	J8704	THEORY OF PLATES & SHELLS	32	31	1

Htno	Subcode	Subname	Internal	External	credits
18BQ1D8710	J8705	PRESTRESSED CONCRETE ELECTIVEI	27	12	0
18BQ1D8710	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	28	31	1
18BQ1D8710	J8711	CAD LABORATORY	32	40	1
18BQ2D6801	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	37	25	1
18BQ2D6801	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	38	29	1
18BQ2D6801	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	38	30	1
18BQ2D6801	J6804	DESIGN FOR TESTABILITY	36	26	1
18BQ2D6801	J6805	DSP PROCESSORS AND ARCHITECTURES	37	27	1
18BQ2D6801	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	36	26	1
18BQ2D6801	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	39	55	1
18BQ2D6802	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	12	0
18BQ2D6802	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	34	14	0
18BQ2D6802	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	34	17	0
18BQ2D6802	J6804	DESIGN FOR TESTABILITY	38	30	1
18BQ2D6802	J6805	DSP PROCESSORS AND ARCHITECTURES	35	26	1
18BQ2D6802	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	35	24	1
18BQ2D6802	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	38	56	1
18BQ2D6803	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	39	30	1
18BQ2D6803	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	39	37	1
18BQ2D6803	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	39	27	1
18BQ2D6803	J6804	DESIGN FOR TESTABILITY	38	34	1
18BQ2D6803	J6805	DSP PROCESSORS AND ARCHITECTURES	40	40	1
18BQ2D6803	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	39	32	1
18BQ2D6803	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	37	58	1
18BQ2D6804	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	-1	0
18BQ2D6804	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	40	-1	0
18BQ2D6804	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	39	-1	0
18BQ2D6804	J6804	DESIGN FOR TESTABILITY	39	-1	0
18BQ2D6804	J6805	DSP PROCESSORS AND ARCHITECTURES	39	-1	0
18BQ2D6804	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	38	-1	0
18BQ2D6804	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	39	-1	0
18BQ2D6805	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	37	27	1
18BQ2D6805	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	36	25	1
18BQ2D6805	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	38	29	1
18BQ2D6805	J6804	DESIGN FOR TESTABILITY	39	24	1
18BQ2D6805	J6805	DSP PROCESSORS AND ARCHITECTURES	38	34	1
18BQ2D6805	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	39	32	1
18BQ2D6805	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	38	57	1
18BQ2D6806	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	39	-1	0
18BQ2D6806	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	33	-1	0
18BQ2D6806	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	33	-1	0
18BQ2D6806	J6804	DESIGN FOR TESTABILITY	36	-1	0
18BQ2D6806	J6805	DSP PROCESSORS AND ARCHITECTURES	35	-1	0
18BQ2D6806	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	35	-1	0
18BQ2D6806	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	32	-1	0
18BQ2D6807	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	25	1
18BQ2D6807	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	38	51	1
18BQ2D6807	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	40	35	1
18BQ2D6807	J6804	DESIGN FOR TESTABILITY	39	34	1
18BQ2D6807	J6805	DSP PROCESSORS AND ARCHITECTURES	39	43	1
18BQ2D6807	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	40	34	1

Htno	Subcode	Subname	Internal	External	credits
18BQ2D6807	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	37	59	1

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **16-11-2019]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]

N. Mohan Rao

Date:02-11-2019

Controller of Examinations